**March 1st Senior Project Meeting**

**Armstrong Hall 148: 2:00PM – 2:45PM**

**Members in Attendance:** All members

* Zach
  + Last Week
    - Uploaded Ian’s PSoC Program
    - Updated chip.v
    - Worked TCF poster
    - Updated schedule
    - Worked with PlanAhead Tutorial
    - Created document for final report
    - Realistic constraints form
    - Xilinx ISE will work
  + Next Week
    - Work with PlanAhead
    - Help finish Ian’s I2S PSoC Program
    - Work on TCF Poster
  + Questions
    - When should we give you a TCF poster draft by?
      * Before break
    - What speed is FPGA? -3, -2, -1
      * Look in the data sheet
    - Can you help with PlanAhead?
      * Will meet with Dr. Pearlstein
    - How do we specify the I/O ports?
      * Will meet with Dr. Pearlstein
* Julie
  + Last Week
    - Looked into EDA tools from Princeton
    - Updated register Verilog code
    - Updated register Excel document
  + Next Week
    - Physical Design
* Dhruvit
  + Last Week
    - Filter model in Java
    - Fixed issues with filter Verilog code
  + Next Week
    - Physical Design
* Kevin
  + Last Week
    - Top-level simulation/verifications
    - I2S debugging
  + Next Week
    - Continue verification
* Whitley
  + Last Week
    - Created multiple test benches with different register values
  + Next Week
    - Continue verification
* Additional Comments
  + Source and sink could come from UDA 1300
  + Might need to buy this